CLAIMS

1. A semiconductor radiation detector comprising a substrate of Si or GaAs, and a CdTe or CdZnTe growth layer laminated and formed on a surface of the substrate by the MOVPE method, wherein the growth layer is an active layer for incident radiation.

2. The semiconductor radiation detector of claim 1, wherein the Si or GaAs substrate is an N-type of low resistance, and the CdTe or CdZnTe growth layer is a P-type of high resistance.

3. The semiconductor radiation detector of claim 2, wherein a thin CdTe or CdZnTe intermediate growth layer of an N-type of low resistance is provided between the Si or GaAs substrate and the CdTe or CdZnTe growth layer.

4. The semiconductor radiation detector of claim 3, wherein grooves extending from the surface side growth layer to the Si or GaAs substrate are provided by cutting means, and separated into multiple unit elements in a two-dimensional arrangement.

5. The semiconductor radiation detector of claim 3, wherein multiple surface electrodes or Schottky electrodes are provided on the surface side growth layer of the semiconductor radiation detector, and guard ring electrodes are provided so as to surround the surface electrodes or Schottky electrodes.

6. The semiconductor radiation detector of claim 3, wherein the low resistance growth layer at the surface side

is divided into multiple small regions, and arranged in a two-dimensional layout, and in the small regions, or in small regions of the Schottky electrode, high voltage can be applied in between a main small region at a specified position and plural peripheral small regions that surround the main small region.

7. The semiconductor radiation detector of claim 1, wherein the Si or GaAs substrate is a P-type of low resistance, and the CdTe or CdZnTe growth layer is formed by laminating the P-type layer of high resistance at a Si or GaAs substrate side and the N-type layer of low resistance at a surface side.

8. The semiconductor radiation detector of claim 7, wherein between a Si or GaAs substrate and the CdTe or CdZnTe growth layer, a thin CdTe or CdZnTe intermediate growth layer of a P-type of low resistance containing arsenic is provided.

9. The semiconductor radiation detector of claim 8, wherein instead of the N-type layer at the surface side, a Schottky electrode is provided.

10. The semiconductor radiation detector of claim 7, wherein instead of the N-type layer at the surface side, a Schottky electrode is provided.

11. The semiconductor radiation detector of claim 7, wherein grooves extending from the surface side growth layer to the Si or GaAs substrate are provided by cutting means, and separated into multiple unit elements in a two-dimensional arrangement.

12. The semiconductor radiation detector of claim 7, wherein multiple surface electrodes or Schottky electrodes are provided on the surface side growth layer of the semiconductor radiation detector, and guard ring electrodes are provided so as to surround the surface electrodes or Schottky electrodes.

13. The semiconductor radiation detector of claim 7, wherein the low resistance growth layer at the surface side is divided into multiple small regions, and arranged in a two-dimensional layout, and in the small regions, or in small regions of the Schottky electrode, high voltage can be applied in between a main small region at a specified position and plural peripheral small regions that surround the main small region.

14. A manufacturing method of a semiconductor radiation detector comprising a Si substrate, and a CdTe or CdZnTe growth layer laminated and formed on a surface thereof by the MOVPE method, using the growth layer as an active layer for incident radiation, wherein the Si substrate is placed in a high temperature reducing atmosphere, a GaAs powder, or GaAs crystals are decomposed, arsenic is deposited on the Si substrate, and the CdTe or CdZnTe growth layer is laminated and formed on the arsenic-deposited surface of the Si substrate.

15. The manufacturing method of the semiconductor radiation detector of claim 14, wherein the Si substrate is an N-type of low resistance, and the CdTe or CdZnTe growth layer is a P-type of high resistance.

16 The manufacturing method of the semiconductor radiation detector of claim 15, wherein between the Si substrate and the CdTe or CdZnTe growth layer, a thin CdTe or CdZnTe intermediate layer of an N-type of low resistance is provided.

17. The manufacturing method of semiconductor radiation detector of claim 14, wherein the Si substrate is a P-type of low resistance, and the CdTe or CdZnTe growth layer is formed by laminating a P-type layer of high resistance at the Si substrate side and an N-type layer of low resistance at the surface side.

18. The manufacturing method of the semiconductor radiation detector of claim 17, wherein between the Si substrate and the CdTe or CdZnTe growth layer, a thin CdTe or CdZnTe intermediate layer of a P-type of low resistance containing arsenic is provided.

19. The manufacturing method of the semiconductor radiation detector of claim 18, wherein, instead of the N type layer at the surface side, a Schottky electrode is provided.

20. The manufacturing method of the semiconductor radiation detector of claim 17, wherein, instead of the N type layer at the surface side, a Schottky electrode is provided.

21. The manufacturing method of the semiconductor radiation detector of claim 14, wherein grooves extending from the growth layer side to the Si substrate are provided by cutting means so as to be separated into multiple unit elements

in a two-dimensional arrangement.

22. The manufacturing method of the semiconductor radiation detector of claim 14, wherein multiple two-dimensional surface electrodes or Schottky electrodes are provided on the surface of the growth layer side, and guard ring electrodes are provided so as to surround the surface electrodes or Schottky electrodes.

23. The manufacturing method of the semiconductor radiation detector of claim 14, wherein the low resistance growth layer of the surface side is divided into multiple small regions, and arranged in a two-dimensional layout, and in the small regions, or in the small regions of Schottky electrodes, high voltage is applied in between a main small region at a specified position and plural peripheral small regions that surround the main small region.